REMARKS

The Office Action dated January 3, 2008 has been reviewed and carefully considered. Claims 5 and 7-11 remain pending, with claim 5 and 7 being the independent claims. Claim 6 has been cancelled without prejudice. Reconsideration of the above-identified application, as amended and in view of the following remarks, is respectfully requested.

Claims 5-11 stand rejected under 35 USC 102(b) as being anticipated by Young (2006/0030084 A1).

As currently amended, claim 5 contains the feature that "the doped source/drain regions and said one of the p-type or n-type doped regions of the PIN diode are provided by the same polycrystalline silicon island and a vertical n-i-p stack is used by using a doped region of the polysilicon thin film transistor for the n-type region." An example of this feature is illustrated in Figures 4-5 of the application wherein the amorphous silicon intrinsic region overlies a part of the n-type doped drain region of thin film transistor as well as overlies a part of the p-type doped source region of thin film transistor in a vertical n-i-p stack.

Young does not teach or imply the feature that the doped source/drain regions and said one of the p-type or n-type doped regions of the PIN diode are provided by the same polycrystalline silicon island and a vertical n-i-p stack is used by using a doped region of

the polysilicon thin film transistor for the n-type region, as specifically claimed in claim 5 of the present invention.

As currently amended, claim 7 contains the feature "wherein a distance between the doped regions is substantially equal to a gap between adjacent thin film transistors." An example of this feature is illustrated in Figure 3 whereby a lateral PIN diode 12 provides certain advantages over the vertical arrangement of the prior art Fig. 2 and that of the Young device for example. Firstly, the vertical arrangement requires a relatively thick amorphous silicon layer, 0.25 - 1.50μm (or .5 to 1.0μm as described in Young, Par. [0071]) for example, in order to ensure that the reverse leakage current is of a low enough value to allow effective operation of the device. Providing a layer having this thickness is relatively difficult and time consuming. In contrast, the distance between the doped contact regions of the photo sensor in Figure 3 is equal to the gap between adjacent TFTs. In this case, the reverse leakage current can be maintained at an acceptably low level by using a thinner intrinsic layer. Advantageously, this intrinsic layer can be formed simply by deposition and patterning.

Young does not teach or imply the feature wherein a distance between the doped regions is substantially equal to a gap between adjacent thin film transistors.

A claim is anticipated only if each and every element recited therein is expressly or inherently described in a single prior art reference. Young cannot be said to anticipate the

present invention, because Young fails to disclose each and every element recited. Accordingly, Claims 5 and 7 are patentable over Young.

Having shown that Young fails to disclose each and every element claimed, applicant submits that the reason for the Examiner's rejection of claims 5 and 7 has been overcome and can no longer be sustained. Applicant respectfully requests reconsideration, withdrawal of the rejection and allowance of claim 5.

With regard to claims 8-11, these claims ultimately depend from claim 5 or 7, which have been shown to be not anticipated and allowable in view of the cited references. Accordingly, claims 8-11 are also allowable by virtue of their dependence from an allowable base claim.

For all the foregoing reasons, it is respectfully submitted that all the present claims are patentable in view of the cited references. A Notice of Allowance is respectfully requested.

Respectfully submitted,

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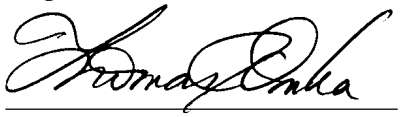

Date: April 2, 2008

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